REMARKS

In this Amendment, Applicant has cancelled Claims 1, 2, 5 – 7 and 20 without prejudice or disclaimer; and amended Claims 3, 4 and 8 – 19; and added new Claims 21 – 27. Claims 3, 4, 8 – 11, 17 and 18 have been amended to overcome the rejections and further specify the embodiments of the present invention. Claims 12 – 16 and 19 have been amended to proper dependent form. It is respectfully submitted that no new matter has been introduced by the amended and new claims. All claims are now present for examination and favorable reconsideration is respectfully requested in view of the preceding amendments and the following comments.

PRIORITY:

Examiner indicates that a certified copy of foreign priority document has not been submitted. Applicant respectfully submits that the certified copy of foreign priority application will be submitted in due course.

OBJECTION TO DRAWINGS:

Figure 1 of the drawing has been objected as failing to identify as "Prior Art."

The corrected drawing sheet has been provided. In the corrected Fig.1, legend of "Prior Art" has been added. Therefore, the objection to the drawing has been overcome and withdrawal of objection is respectfully requested.

CLAIM OBJECTION:

Claims 1, 9 and 20 have been objected as containing informalities.

It is respectfully submitted that the objection has been overcome by the amendment. At first, Claims 1 and 20 have been cancelled. The rejection to these claims is moot. In addition, the proper terms "input interface" and "output interface" have been

used in amended Claim 3. Furthermore, Claim 9 has been amended to depend on Claim 8 and corrected informalities according to Examiner's suggestion. Therefore, the objection to Claims 1, 9 and 20 has been overcome and withdrawal of objection is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 112 FIRST PARAGRAPH:

Claims 3 – 9 and 17 – 20 have been rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement.

It is respectfully submitted that in view of the amendments, the rejection has been overcome. At first, Claims 5 – 7 and 20 have been cancelled. Therefore, the rejection to these claims is moot. In addition, Claim 3 has been amended to further specify the embodiment of the present invention. Applicant respectfully submits that the embodiments of the present invention as in Claims 3 – 4, 8 – 9 and 17 – 19 are enabled to a person of ordinary skill in the art. The Examiner raises concern on the term "while the user control program continues to perform control functions." It is respectfully submitted that a multitasking operation system, such as Microsoft Windows, can be understood by a person of ordinary skill in the art as capable of performing many tasks at the same time. It does not do so in the strictest sense of "at the same time", even though it is called multitasking. It performs one task exclusively for a short time, then switches to another, then another, thus quickly switching between all the necessary tasks to do everything within the required time. However, Windows can be considered capable of performing many tasks at the same time in the sense that it responds to task inputs, and provides the processing service and task outputs sufficiently quickly that the task user is unaware that the system may have broken off from serving the user's task to do something else before finishing the user's task. The multitasking operation system is performing many tasks *apparently* at the same time. The actual cyclic nature of the preferred embodiment including a logic processing interval and the data access interval is described in the application.

The issue with respect of the language of the claims is whether the controller responds quickly enough to new inputs from the process under control and provides new output values as required within an acceptable time frame. The only condition required to satisfy the wording "continue to perform control functions" is that the control read the inputs and supplies the necessary updates to the outputs within the time acceptable for the plant/machinery under control. If it does that, the controlled item remains under control, and does not know or care that the control may have been temporarily occupied on other tasks. The preferred embodiment described in the application achieves this level of continuing control. The term "while the user control program continues to perform control functions" is specifically intended to include both sequential and simultaneous access to state data. The specification includes a section dealing with Build-in means of access (page 17, line 33 – page 18, line 7). This is not the way the preferred embodiment of the present invention operates but the method is still available and a practical way of implementing this aspect if the invention, without any data access interval in the run cycle. It is respectfully submitted that a person of ordinary skill in the art is able to make and use the present invention as amended based on the disclosure of the specification.

Therefore, the rejection under 35 U.S.C. § 112, first paragraph has been overcome. Accordingly, withdrawal of the rejections under 35 U.S.C. § 112, first paragraph, is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102:

Claims 1 – 2 and 10 – 14 have been rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by Vasko (US 6,463,339), hereinafter Vasko.

Applicant traverses the rejection and respectfully submits that the presently claimed invention is not anticipated by the cited reference. At first, Claims 1 – 2 have been cancelled. The rejection to these claims is moot. In addition, the amended Claims 10 – 14 include features that are not disclosed or suggested in Vasko.

It is respectfully submitted that the abstract of Vasko refers to the use of low complexity FPGAs. Vasko mentions nothing more than simple combinational logic or ladder diagram logic throughout the patent in the context of low complexity FPGAs. The complete absence of any reference to a clock, registers, flip-flops, or similar means and the use of anything more complex than straight Boolean combinational logic cannot be assumed. Vasko associates error-detecting circuit with a program circuit implemented in an FPGA. However, Vasko does not teach any method or means of implementing the program circuit other than describing it as a Boolean logic equivalent of a ladder diagram.

Vasko describes the program circuit as being implemented with AND and OR gates, and other combinational logic. There is no mention anywhere in Vasko of the use of flip-flops, sampling and storing values, or more complex functions. Vasko talks purely of the program circuit as a Boolean equivalent of a ladder logic diagram. The focus of Vasko is on the error handling rather than the program circuit. However, Vasko makes no mention of display and modification of state data. It does not describes a user program that has any state data, nor can a user program consisting of combinational logic be said to be capable of running, pausing and stopping.

There are no features of Vasko's program circuit that distinguish it from any other simple combinational logic circuit configured in an FPGA by any other FPGA user. It is just a combinational logic circuit, and Vasko ignores any special features or functions of it other than those related to the use of two differently derived and implemented but functionally equivalent program circuits for the purpose of error handling.

In addition, the issue of input registers, flip-flops and state data, and the absence of any mention of them is Vasko is important. Settled signals cannot be assumed in Vasko because flip-flops and registers are not described and cannot be assumed. Without the use of an input register, the output signals, which are all derived from process inputs, could exhibit glitches at any time. Vasko's error detecting circuit could be modified to ignore glitches of less than a certain time length, but it is indeterminate as to how long they would persist and this is not disclosed.

The completely asynchronous nature of Vasko's circuit is further emphasized by the two different program circuit implementations, which will produce glitches on the error outputs, that is, false output values. In addition, because the implementation is asynchronous and the controlled process necessarily undefined, there are no time intervals during which the error output can be known to accurately reflect the error status of the circuit. Raising the alarm must be done on the basis of the error signal being true for longer than a certain amount of time. That could be inaccurate because rapidly changing inputs could make the false error condition persist for an indeterminate length of time. This is not the case with the clocked synchronous operation described and claimed in the present invention. It is not possible to implement a user program circuit with state data without flip-lops (state data is stored in flip-flops of one kind or another), or displayed and modified state data without at least sampling and storing the PLDPC input and output data using flip-flops. There is no consideration of user circuit state data in Vasko.

Vasko does not disclose a control having the input registers in Claim 3 as amended. Similarly, the input registers and identical user control program circuits of Claims 10 – 11 are not disclosed in Vasko. Without these features, data display and modification, and error handling cannot be properly implemented.

Therefore, the newly presented claims are not anticipated by Vasko and the rejection under 35 U.S.C. § 102 (b) has been overcome. Accordingly, withdrawal of the rejection under 35 U.S.C. § 102 (b) is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 103:

Claims 15 – 16 have been rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Vasko in view of Spiller (US 5,057,994), hereinafter Spiller.

Applicant traverses the rejection and respectfully submits that the embodiments of present-claimed invention are not obvious over Vasko in view of Spiller. As stated above, there are significant differences between the Vasko and the present invention.

Therefore, there is no motivation or suggestion to combine Vasko and Spiller to achieve the present invention. Even if they are combined, a person of ordinary skill in the art will not discern the present invention at time of its invention.

Therefore, the newly presented claims are not obvious over Vasko in view of Spiller and the rejection under 35 U.S.C. § 103 has been overcome. Accordingly, withdrawal of the rejections under 35 U.S.C. § 103 is respectfully requested.

Having overcome all outstanding grounds of rejection, the application is now in condition for allowance, and prompt action toward that end is respectfully solicited.

Respectfully submitted,

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Amendments to the Drawings:

The attached sheet of drawing includes changes to Fig.1. This sheet, which includes Fig. 1, replaces the original sheet including Fig. 1. In Fig. 1, legend of "Prior Art" has been added.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

Annotated Sheet Showing Changes

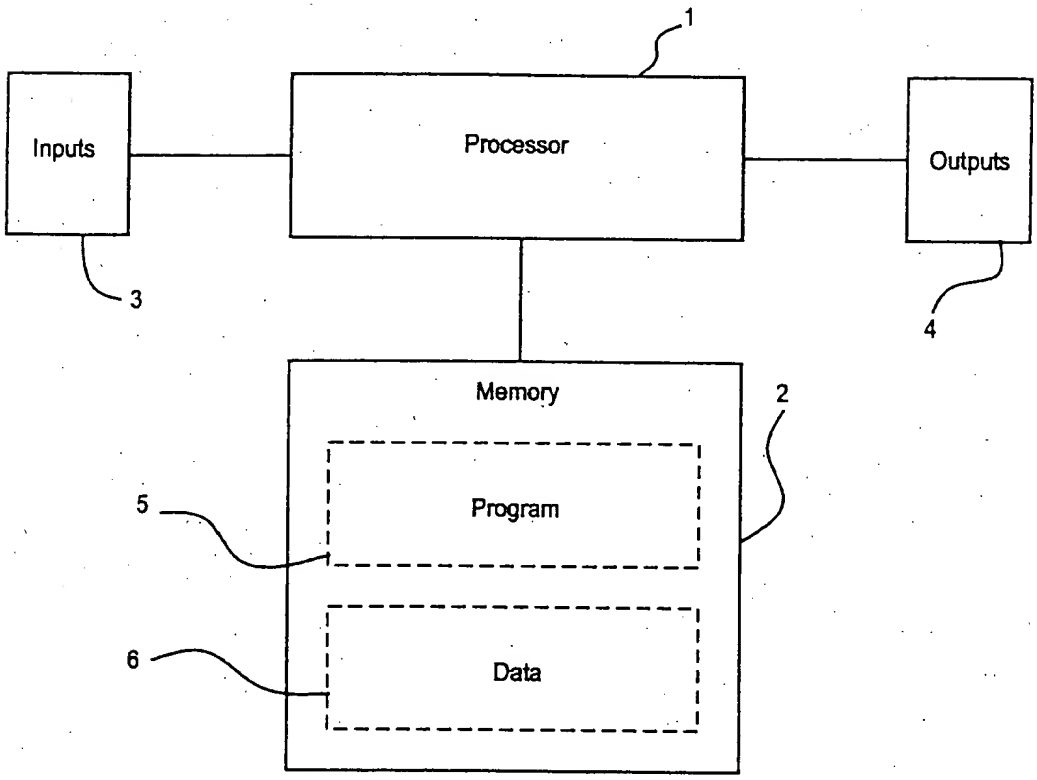

Fig. 1 (Prior Art)